AC6951G Datasheet

Zhuhai Jieli Technology Co.,LTD

Version：V1.0

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AC6951G Features

CPU

- 32-bit DSP supports hardware Float Point Unit (FPU)
- Up to 240MHz programmable processor
- 64Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Acoustic echo cancellation/suppression (AEC,AES)
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 30-band EQ configuration for voice Effects

Audio Codec

- Two channels 16-bit DAC, SNR >= 92dB
- Three channels 16-bit ADC , SNR >= 90dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/ 32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias generator
- Supports two PDM digital MIC inputs
- three channels Stereo analog MUX
- Supports cap-less, single-ended, and differential mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Peripherals

- One full speed USB 2.0 OTG controller
- Two PCM/IIS for external digital Audio code, supports host and device mode
- Four multi-function 16-bit timers, support capture and PWM mode
- Three 16-bit PWM generator for motor driving
- Three full-duplex basic UART, UART0 and UART1 supports DMA mode
- Three SPI interface supports host and device mode
- Two SD Card Host controller
- One hardware IIC interface supports host and device mode
- Four SPDIF receiving interface without analog amplify. Supports DTS/PCM format. supports Sample rate of 8KHz~192KHz. Up to 24-bit resolution.
- Supports HDMI ARC (Audio Return Channel) receiving.
- Segment LCD panels
- Digital matrix LED panels
- Built-in Cap Sense Key controller
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

PMU

- Low voltage LDO for internal digital and analog circuit supply
- 3uA current consumption in the soft-off mode
- Built-in LDO for core, IO,flash.
- VBAT is 2.2V to 5.5V
- VDDIO is 2.2V to 3.6V
- RTCVDD is 2.2V to 3.6V

Packages

- LQFP48(7mm*7mm)

Temperature

- Operating temperature: -20℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Sound Box

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1、Pin Definition

1.1 Pin Assignment

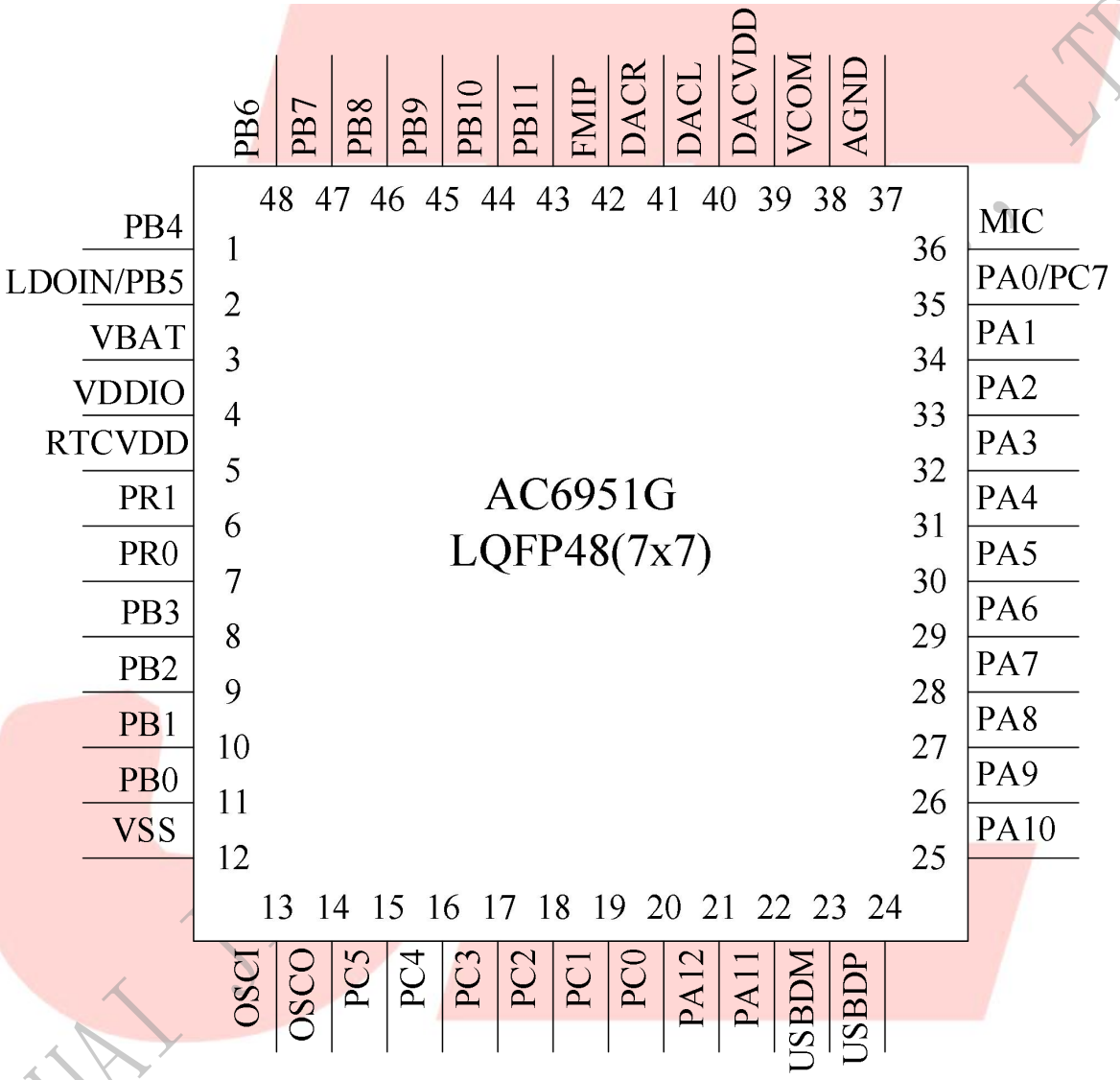


Figure 1-1 AC6951G Package Diagram

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1.2 Pin Description

Table 1-1 AC6951G Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	PB4	I/O	24/8	GPIO	SD1DAT0B：SD1 Data0(B); SD0DAT3B：SD0 Data3(B); IIC_SCL_C：IIC SCL(C); ADC7：ADC Input Channel 7; UART0TXB：Uart0 Data Out(B); LVD：Low Voltage Detect Input; PWMCH2H：Motor PWM Channel2 (H);
2	LDOIN	P	/		Battery Charge Input;
	PB5	I/O	8	GPIO (High Voltage Resistance)	SD1CMDB：SD1 Command(B); SD0DAT2B：SD1 Data2(B); PWM3：Timer3 PWM Output; CAP1：Timer1 Capture; UART0TXC：Uart0 Data Out(C); UART0RXC：Uart0 Data In(C);
3	VBAT	P	/		Power Supply
4	VDDIO	P	/		IO Power 3.3v
5	RTVDDD	P	/		RTC Power Supply
6	PR1	I/O	/	RTCIO1	OSCO_32K
7	PR0	I/O	/	RTCIO0	OSCI_32K
8	PB3	I/O	24/8	GPIO	PWM2：Timer2 PWM Output; ADC6：ADC Input Channel 6; Q-Decoder1_1;
9	PB2	I/O	8	GPIO (High Voltage Resistance)	SPI1DIA：SPI1 Data In(A); Q-Decoder1_0; PWMCH1L：Motor PWM Channel1 (L)；
10	PB1	I/O	24/8	GPIO (pull up)	Long Press Reset； SPI1DOA：SPI1 Data Out(A); ADC5：ADC Input Channel 5; TMR2：Timer2 Clock Input; UART1RXA：Uart1 Data In(A); SPDIF_IN_D：Sony/Philips Digital Interface Input(D)

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11	PB0	I/O	8	GPIO (High Voltage Resistance)	SPI1CLKA：SPI1 Clock(A); ALNK1_MCLK：ALNK1 Master Clock; SPDIF_IN_C：Sony/Philips Digital Interface Input(C) UART1TXA：Uart1 Data Out(A); PWMCH1H：Motor PWM Channel1(H)；
12	VSS	G	/		Digital Ground
13	OSCI	I	/		OSC In
14	OSCO	O	/		OSC Out
15	PC5	I/O	24/8	GPIO	SD1CLKA：SD1 Clock(A); SPI1DOB：SPI1 Data Out(B); UART2RXD：Uart2 Data In(D); IIC_SDA_B：IIC SDA(B); ALNK1_DAT3：Audio Link Data3; ADC13：ADC Input Channel 13; COM0：LCD COM Output 0; PAPD7：PAP Data 7; Touch15：Touch Input Channel 15; PWMCH5L：Motor PWM Channel5(L)；
16	PC4	I/O	24/8	GPIO	SD1CMDA：SD1 Command(A); SPI1CLKB：SPI1 Clock(B); UART2TXD：Uart2 Data Out(D); IIC_SCL_B：IIC SCL(B); ALNK1_DAT2：Audio Link Data2; ADC10：ADC Input Channel 10; COM1：LCD COM Output 1; PAPD6：PAP Data 6; Touch14：Touch Input Channel 14; PWMCH5H：Motor PWM Channel5(H)；
17	PC3	I/O	24/8	GPIO	SD1DAT0A：SD1 Data0(A); SPI1DIB：SPI1 Data In(B); ALNK1_DAT1：Audio Link Data1; COM2：LCD COM Output 2; PAPD5：PAP Data 5; Touch13：Touch Input Channel 13;
18	PC2	I/O	24/8	GPIO	SD1DAT1A：SD1 Data1(A); ALNK1_DAT0：Audio Link Data0; COM3：LCD COM Output 3; SEG18：LCD SEG Output18; PAPD4：PAP Data 4; Touch12：Touch Input Channel 12; FPIN5：Motor Auto-Stop Protective Pin5；

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19	PC1	I/O	24/8	GPIO	SD1DAT2A：SD1 Data2(A); ALNK1_LRCK：Audio Link Word Select; COM4：LCD COM Output 4; SEG17：LCD SEG Output17; PAPD3：PAP Data 3; Touch11：Touch Input Channel 11; UART1RXB：Uart1 Data In(B); FPIN4：Motor Auto-Stop Protective Pin4；
20	PC0	I/O	24/8	GPIO	SD1DAT3A：SD1 Data3(A); ALNK1_SCLK：Audio Link Serial Clock; COM5：LCD COM Output 5; SEG16：LCD SEG Output16; PAPD2：PAP Data 2; Touch10：Touch Input Channel 10; UART1TXB：Uart1 Data Out(B); FPIN3：Motor Auto-Stop Protective Pin3；
21	PA12	I/O	24/8	GPIO	PWM1：Timer1 PWM Output; ALNK0_DAT1B：Audio Link Data1(B); ADC4：ADC Input Channel 4; SEG12：LCD SEG Output12; PAPWR：PAP Write Clock; UART0RXD：Uart0 Data In(D);
22	PA11	I/O	24/8	GPIO	ALNK0_DAT0B：Audio Link Data0(B); SEG11：LCD SEG Output11; PAPRD：PAP Read Clock; UART0TXD：Uart0 Data Out(D);
23	USBDM	I/O	4	USB Negative Data (pull down)	UART1RXD：Uart1 Data In(D); SPI2DOB：SPI2 Data Out(B); IIC_SDA_A：IIC SDA(A);
24	USBDP	I/O	4	USB Positive Data (pull down)	UART1TXD：Uart1 Data Out(D); SPI2CLKB：SPI2 Clock(B); IIC_SCL_A：IIC SCL(A); ADC12：ADC Input Channel 12;
25	PA10	I/O	24/8	GPIO	SD0CLKA：SD0 Clock(A); ALNK0_LRCKB：Audio Link Word Select(B); ADC3：ADC Input Channel 3; SPDIF_IN_B：Sony/Philips Digital Interface Input(B) TMR1：Timer1 Clock Input; SEG10：LCD SEG Output10; PAPD1：PAP Data 1; Touch9：Touch Input Channel 9; UART2RXB：Uart2 Data In(B); PWMCH4L：Motor PWM Channel4(L)；

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26	PA9	I/O	24/8	GPIO	SD0CMA：SD0 Command(A); ALNK0_SCLKB：Audio Link Serial Clock(B); SPDIF_IN_A：Sony/Philips Digital Interface Input(A) SEG9：LCD SEG Output9; PAPD0：PAP Data 0; Touch8：Touch Input Channel 8; UART2TXB：Uart2 Data Out(B); PWMCH4H：Motor PWM Channel4(H)；
27	PA8	I/O	24/8	GPIO	SD0DAT3A：SD0 Data3(A); ALNK0_MCLKA：ALNK Master Clock(A); SEG8：LCD SEG Output8; BT_Freq; FPIN2：Motor Auto-Stop Protective Pin2；
28	PA7	I/O	24/8	GPIO	SD0DAT2A：SD0 Data2(A); ALNK0_DAT3A：Audio Link Data3(A); SEG7：LCD SEG Output7; BT_priority; TMR0：Timer0 Clock Input; Touch7：Touch Input Channel 7;
29	PA6	I/O	24/8	GPIO	SD0DAT1A：SD0 Data1(A); ALNK0_DAT2A：Audio Link Data2(A); ADC2：ADC Input Channel 2; Wlan_Active; IIC_SDA_D：IIC SDA(D); SEG6：LCD SEG Output6; Touch6：Touch Input Channel 6; UART0RXA：Uart0 Data In(A);
30	PA5	I/O	24/8	GPIO	SD0DAT0A：SD0 Data0(A); ALNK0_DAT1A：Audio Link Data1(A); ADC1：ADC Input Channel 1; BT_Active; IIC_SCL_D：IIC SCL(D); SEG5：LCD SEG Output5; Touch5：Touch Input Channel 5; PWM0：Timer0 PWM Output; UART0TXA：Uart0 Data Out(A);
31	PA4	I/O	24/8	GPIO	ALNK0_DAT0A：Audio Link Data0(A); SEG4：LCD SEG Output4; Touch4：Touch Input Channel 4;

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32	PA3	I/O	24/8	GPIO	PLNK_DAT1：PLNK Data1; ALNK0_LRCKA：Audio Link Word Select(A); SEG3：LCD SEG Output3; Touch3：Touch Input Channel 3; UART2RXA：Uart2 Data In(A); Q-Decoder0_1;
33	PA2	I/O	24/8	GPIO	PLNK_SCLK：PLNK Serial Clock; ALNK0_SCLKA：Audio Link Serial Clock(A); SEG2：LCD SEG Output2; Touch2：Touch Input Channel 2; UART2TXA：Uart2 Data Out(A); Q-Decoder0_0; CAP3：Timer3 Capture;
34	PA1	I/O	24/8	GPIO	AMUX0R：Analog Channel0 Right; SEG1：LCD SEG Output1; Touch1：Touch Input Channel 1; ADC0：ADC Input Channel 0; UART1RXC：Uart1 Data In(C); PWMCH0L：Motor PWM Channel0(L)；
35	PA0	I/O	24/8	GPIO	AMUX0L：Analog Channel0 Left; SEG0：LCD SEG Output0; Touch0：Touch Input Channel 0; CLKOUT0; UART1TXC：Uart1 Data Out(C); PWMCH0H：Motor PWM Channel0(H)；
	PC7	I/O	/	GPIO	MIC_BIAS：Microphone Bias Output SEG21：LCD SEG Output21;
36	MIC	I	/		MIC：MIC Input Channel;
37	AGND	G	/		Analog Ground
38	VCOM	P	/		DAC Reference
39	DACVDD	P	/		DAC Power
40	DACL	O	/		DAC Left Channel
41	DACR	O	/		DAC Right Channel
42	FMIP	I	/		FM Single Input
43	PB11	I/O	/	GPIO	SDPG：SD Card Power Gate;
44	PB10	I/O	24/8	GPIO	AMUX2R：Analog Channel2 Right; SD0CMB：SD0 Command(B); SPI2DOA：SPI2 Data Out(A); SD1DAT3B：SD1 Data3(B); ADC9：ADC Input Channel 9; UART2RXC：Uart2 Data In(C); PWMCH3L：Motor PWM Channel3(L)；

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45	PB9	I/O	24/8	GPIO	AMUX2L：Analog Channel2 Left; SD0CLKB：SD0 Clock(B); SPI2CLKA：SPI2 Clk(A); SD1DAT2B：SD1 Data2(B); CAP0：Timer0 Capture; UART2TXC：Uart2 Data Out(C); PWMCH3H：Motor PWM Channel3(H)；
46	PB8	I/O	24/8	GPIO	AMUX1R：Analog Channel1 Right; SD0DAT0B：SD0 Data0(B); SPI2_DIA：SPI2 Data In(A); SD1DAT1B：SD1 Data1(B); ADC8：ADC Input Channel 8; CLKOUT1：Clk Out1;
47	PB7	I/O	24/8	GPIO	AMUX1L：Analog Channel1 Left;
48	PB6	I/O	24/8	GPIO	SD1CLKB：SD1 Clock(B); SD0DAT1B：SD0 Data1(B); IIC_SDA_C：IIC SDA(C); TMR3：Timer3 Clock Input; UART0RXB：Uart0 Data In(B); PWMCH2L：Motor PWM Channel2 (L)；

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2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-20	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	+5.5	V
LDOIN	Charger Voltage	-0.3	+6.0	V
$V_{3.3IO}$	3.3V IO Input Voltage	-0.3	+3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	5.5	V	_
LDOIN	Charger Voltage	4.5	5.0	5.5	V	_
V_{DDIO33}	Voltage output	_	3.3	_	V	VBAT = 5V, 100mA loading
V_{DACVDD}	DAC Voltage	_	2.7	_	V	VBAT = 5V, 10mA loading
$I_{VDDIO33}$	Loading current	_	_	150	mA	VBAT = 5V

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDOIN	Charge Input Voltage	4.5	5	6.0	V	_
V_{Charge}	Charge Voltage	4.15	4.2	4.25	V	_
I_{Charge}	Charge Current	20	_	300	mA	Charge current at fast charge mode
I_{Trikl}	Trickle Charge Current	20	45	70	mA	$V_{BAT}<V_{Trikl}$

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2.4 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	High-Level Input Voltage	0.7* VDDIO	–	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V_{OL}	Low-Level Output Voltage	–	–	0.33	V	VDDIO = 3.3V
V_{OH}	High-Level Output Voltage	2.7	–	–	V	VDDIO = 3.3V

2.5 Internal Resistor Characteristics

Table 2-4

Port		**General Output**	**High Drive**	**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
PA0~PA12 PB1, PB3, PB4, PB6~PB10 PC0~PC5		8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、PB0, PB2, PB5 can pull-up resistance to 5V 4、internal pull-up/pull-down resistance | accuracy ±20% 5、PRx supply by RTCVDD
PB11 PC7	Output 0	8mA	24mA	10K	10K	
	Output 1	8mA	64mA			
PB0, PB2, PB5		8mA	–	10K	10K	
PR0-PR1		8mA	–	10K	10K	
USBDP		4mA	–	1.5K	15K	
USBDM		4mA	–	180K	15K	

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2.6 DAC Characteristics

Table 2-5

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	_	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	_	-75	_	dB	
S/N	_	92	_	dB	
Crosstalk	_	-80	_	dB	
Output Swing		1		Vrms	
Dynamic Range	_	90	_	dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power	11	_	_	mW	32ohm loading

2.7 ADC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		80		dB	1KHz/-60dB
S/N	_	90	91	dB	1KHz/-60dB
THD+N	_	-70	_	dB	
Crosstalk	_	-80	_	dB	

2.8 FM Receiver Characteristics

Table 2-11

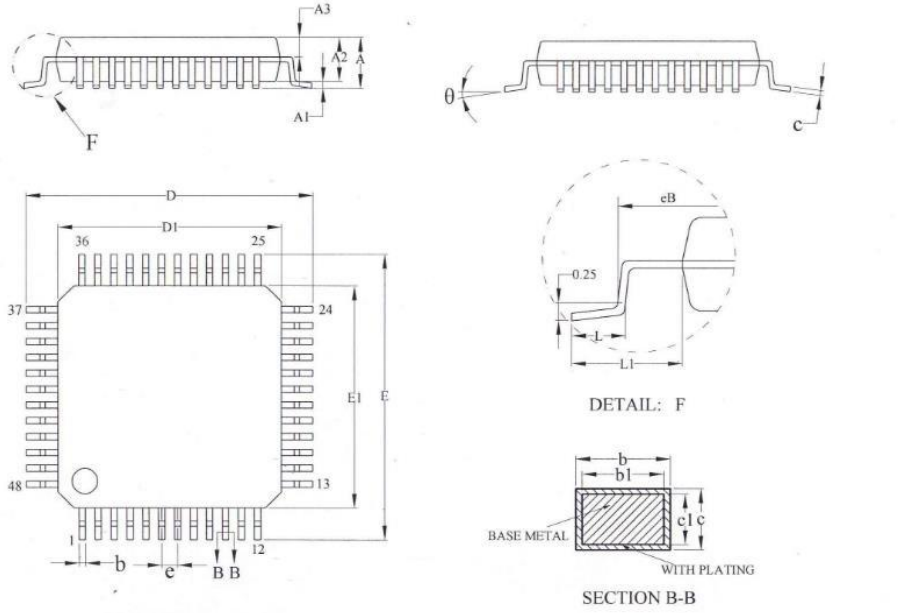
Parameter	Min	Typ	Max	Unit	Test Conditions
Input Frequency	76		108	MHz	
Usable Sensitivity	3	4	8	dBμV EMF	(S+N)/N=26dB
Adjacent Channel Selectivity	_	48	_	dB	± 200kHz
IIP3	_	88	_	dbμV EMF	Δ f1=200 kHz, Δ f2=400 kHz
Audio Output Voltage	0	_	3	V	Empty Load
Audio Frequency Response	20	_	20k	Hz	DacTest
Audio (S+N)/N	_	58	_	dB	
Stereo Separation	_	40	_	dB	
Audio Total Harmonic Distortion (THD)	_	0.4	_	%	

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3、Package Information

3.1 LQFP48(7mm*7mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.50BSC		
L	0.40	—	0.65
L1	1.00REF		
θ	0	—	7°

Figure 3-1. AC6951G Package

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4、Revision History

Date	Revision	Description
2020.10.30	V1.0	Initial Release

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